WHAT IS CLAIMED IS:

1. A method for manufacturing a package substrate without using any plating lead line, comprising the steps of:

a) laminating first dry films over upper and lower surfaces of a base substrate having via holes plated with a copper film and being formed at the upper and lower surfaces thereof with copper foils, and subjecting the first dry films to exposure and development processes, thereby exposing predetermined upper and lower surface portions of the base substrate;

b) removing portions of the copper foils not covered by the first dry films in accordance with an etching process, thereby forming circuits on the upper and lower surfaces of the base substrate, respectively;

c) stripping the first dry films, and forming a plated layer over all portions of the base substrate in accordance with an electroless plating process;

d) laminating second dry films over the plated upper and lower surfaces of the base substrate, and subjecting the second dry films to exposure and development processes, thereby exposing portions of the plated upper and lower surfaces of the base substrate respectively corresponding to regions where Au is to be plated;

e) removing the plated layer from the exposed upper and

lower surface portions of the base substrate respectively corresponding to the regions where Au is to be plated, in accordance with an etching process;

f) plating Au on the exposed upper and lower surface portions of the base substrate;

g) stripping the second dry films, and removing the plated layer remaining on the base substrate in accordance with an etching process, thereby exposing the upper and lower circuits of the base substrate; and

h) coating a solder resist on the exposed upper and lower circuits of the base substrate while exposing predetermined portions of the upper and lower circuits.

2. The method according to claim 1, wherein the first and second dry films are used as etch resists, respectively.

3. The method according to claim 1, wherein the electroless plating process is carried out by chemically plating a conductor in a state in which bus lines of the upper and lower circuits are completely removed after completion of the etching process at the step (b).

4. The method according to claim 3, wherein the conductor is a copper layer having a thickness of 0.5 to 1.0μm.

5. The method according to claim 1, wherein each of the etching processes is a flash etching process.

6. The method according to claim 1, wherein the plated layer formed in the electroless plating process is a conductor serving as a plating lead line for supplying current during an electrolytic plating process for the plating of Au.

7. The method according to claim 1, wherein the exposed upper surface portions of the base substrate respectively corresponding to the regions where Au is to be plated are bond fingers.

8. The method according to claim 1, wherein the exposed lower surface portions of the base substrate respectively corresponding to the regions where Au is to be plated are solder ball pads.

9. A method for plating Au on a package substrate, comprising the steps of:

a) laminating first dry films over upper and lower surfaces of a base substrate having via holes plated with a copper film and being formed at the upper and lower surfaces thereof with copper foils, and subjecting the first dry films to exposure and development processes, thereby exposing

predetermined upper and lower surface portions of the base substrate;

b) removing portions of the copper foils not covered by the first dry films in accordance with an etching process, thereby forming circuits on the upper and lower surfaces of the base substrate, respectively;

c) stripping the first dry films, and forming a plated layer over all portions of the base substrate in accordance with an electroless plating process;

d) laminating second dry films over the plated upper and lower surfaces of the base substrate, and subjecting the second dry films to exposure and development processes, thereby exposing portions of the plated upper and lower surfaces of the base substrate respectively corresponding to regions where Au is to be plated;

e) removing the plated layer from the exposed upper and lower surface portions of the base substrate respectively corresponding to the regions where Au is to be plated, in accordance with an etching process; and

f) plating Au on the exposed upper and lower surface portions of the base substrate, whereby the base substrate is plated with Au without using any plating lead line.

10. The method according to claim 9, wherein the electroless plating process is carried out by chemically

plating a conductor in a state in which bus lines of the upper and lower circuits are completely removed after completion of the etching process at the step (b).

11. The method according to claim 10, wherein the conductor is a copper layer having a thickness of 0.5 to 1.0μm.

12. The method according to claim 9, wherein each of the etching processes is a flash etching process.

13. The method according to claim 9, wherein the plated layer formed in the electroless plating process is a conductor serving as a plating lead line for supplying current during an electrolytic plating process for the plating of Au.

14. A method for electrolytically plating Au on a package substrate without using any plating lead line, comprising the steps of:

a) laminating first dry films over upper and lower surfaces of a base substrate having via holes plated with a copper film and being formed at the upper and lower surfaces thereof with copper foils, and subjecting the first dry films to exposure and development processes, thereby exposing predetermined upper and lower surface portions of the base substrate;

b) removing portions of the copper foils not covered by the first dry films in accordance with an etching process, thereby forming circuits on the upper and lower surfaces of the base substrate, respectively;

c) stripping the first dry films, and forming a plated layer over all portions of the base substrate in accordance with an electroless plating process;

d) laminating second dry films over the plated upper and lower surfaces of the base substrate, respectively and subjecting the second dry film laminated over the plated upper surface of the base substrate to exposure and development processes, thereby exposing predetermined portions of the plated upper surface of the base substrate, while tenting the via holes;

e) removing the plated layer from the exposed upper surface portions of the base substrate in accordance with an etching process;

f) laminating a third dry film over an upper surface of a structure obtained after completion of the step (e), subjecting the third dry film to exposure and development processes, thereby exposing portions of the upper surface of the base substrate respectively corresponding to regions where Au is to be plated, and plating Au on the exposed upper surface portions of the base substrate;

g) stripping the second dry film laminated on the lower

surface of the substrate, and the third dry film remaining on the upper surface of the structure, and removing the plated layer remaining on the lower surface of the base substrate in accordance with an etching process, thereby exposing the upper and lower circuits of the base substrate;

h) coating a solder resist over the exposed upper and lower circuits of the base substrate, and subjecting the solder resist to exposure and development processes, thereby exposing predetermined portions of the upper and lower circuits; and

i) surface-treating the exposed portions of the lower circuit by use of an organic solderability preservative agent.

15. A package substrate plated with Au in accordance with an electrolytic Au plating process using no plating lead line, comprising:

a base substrate formed with a plurality of via holes;

a first plated layer formed on predetermined portions of the base substrate and respective inner surfaces of the via holes to form circuit patterns at upper and lower surfaces of the base substrate, respectively, the first plated layer being made of copper;

a second plated layer formed on predetermined portions of the circuit patterns in accordance with an electroless plating process;

an Au plated layer formed on portions of the circuit

patterns corresponding to regions where the second plated layer is not present; and

a solder resist coated on the circuit patterns, except for the Au plated layer thereof.

16. The package substrate according to claim 15, wherein the second plated layer is a conductor chemically plated in an electroless manner in a state in which bus lines of the upper and lower circuits are completely removed.

17. The package substrate according to claim 16, wherein the conductor is a copper layer having a thickness of 0.5 to 1.0μm.

18. The package substrate according to claim 15, wherein the second plated layer serves as a plating lead line for supplying current during an electrolytic plating process for the formation of the Au plated layer.